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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte G.R. MOHAN RAO

Appeal 2008-0501
Application 10/665,906
Technology Center 2100

Decided:[1] April 7, 2009

Before ALLEN R. MACDONALD, *Vice Chief Administrative Patent Judge*, HOWARD B. BLANKENSHIP, and ST. JOHN COURTENAY, *Administrative Patent Judges*.

MACDONALD, *Vice Chief Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Data (electronic delivery).

STATEMENT OF CASE

Introduction

Appellant appeals under 35 U.S.C. § 134 from a non-final rejection of claims 1-21 mailed October 20, 2006. We have jurisdiction under 35 U.S.C. § 6(b).

According to Appellant, the present inventive concepts are embodied in a switch comprising a plurality of ports for exchanging data words of a predetermined word-width, or variable word-width, and a shared-memory for enabling the exchange of data between first and second ones of the ports. (Spec. ¶ [0010]).

Exemplary Claim(s)

Exemplary independent claims 1 and 8 under appeal reads as follows:

1. A switch comprising:

> a plurality of ports for exchanging data, and a shared-memory for enabling the exchange of data between first and second ones of said ports, said shared-memory comprising:
>
> an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width;
>
> circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports.

18. A shared-memory switch comprising:

a plurality of ports for exchanging data between external devices associated with each of said ports;

a buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words;

a shared-memory for effectuating a transfer of data from a first one of said ports to a second one of said ports through corresponding ones of said buffers, said shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of said predetermined width and circuitry for selecting a row in response to a received address;

a plurality of available address tables each for maintaining a queue of addresses available for writing said single words of data to a corresponding one of said banks; and

a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of said banks.

Prior Art

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Joffe	US 5,440,523	Aug. 8, 1995
Mathur	US 6,424,658 B1	Jul. 23, 2002

Rejections

1. The Examiner rejected claims 1-21 under 35 U.S.C. § 112, second paragraph, as being indefinite.

2. The Examiner rejected claims 1, 2, 7, 16, and 17 under 35 U.S.C. § 102(b) as being anticipated by Joffe.

3. The Examiner rejected claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Joffe.

4. The Examiner rejected claims 1-3, 5-8, 10-17, and 20 under 35 U.S.C. § 102(b) as being anticipated by Mathur.

5. The Examiner rejected claims 4, 9, 18, 19, and 21 under 35 U.S.C. § 103(a) as being unpatentable over Mathur.

Appellant's Contentions

1. Appellant contends that the Examiner erred in rejecting claims 1-21, as being indefinite because claims 1-21 meet the requirements of 35 U.S.C. § 112, second paragraph (App. Br. 4-7).

2. Appellant contends that the Examiner erred in rejecting claims 1, 2, 7, 16, and 17 under 35 U.S.C. § 102(b) as being anticipated by Joffe, claims 3 and 4 under 35 U.S.C. § 103(a) as being obvious over Joffe, claims 1-3, 5-8, 10-17, and 20 under 35 U.S.C. § 102(b) as being anticipated by Mathur, and claims 4, 9, 18, 19, and 21 under 35 U.S.C. § 103(a) as being obvious over Mathur, because:

(A) repeatedly "the Examiner has not provided . . . objective evidence" to show claimed features (e.g., App. Br. 11) and has rejected other features "without providing any evidence" (e.g., App. Br. 16), and

(B) because Joffe and Mathur lack teachings of many of the limitations required by claims 1-21 (App. Br. 7-37).

3. Appellant contends that the Examiner erred in rejecting claims 4, 9, 18, 19, and 21 under 35 U.S.C. § 103(a) as being obvious over Mathur, because a suggestion or motivation is required to make a rejection under 35 U.S.C. § 103 over Mathur (App. Br. 32-37).

Result

We affirm-in-part, vacate-in-part, and enter a new ground of rejection.

ISSUE(S)

(1)

Whether Appellant has shown that the Examiner erred in rejecting claims 1-21, because the claims are definite as required under 35 U.S.C. § 112, second paragraph?

(2)

Whether Appellant has shown that the Examiner erred in rejecting claims 1-21 because repeatedly "the Examiner has not provided . . . objective evidence" to show claimed features (e.g., App. Br. 11) and has rejected other features "without providing any evidence" (e.g., App. Br. 16)?

(3)

Whether Appellant has shown that the Examiner has erred in rejecting claims 1-21 because Joffe and Mathur lack teachings of nearly all the limitations required by claims 1-21?

(4)

Whether Appellant has shown that the Examiner has erred in rejecting claims 4, 9, 18, 19, and 21 over Mathur because a teaching, suggestion, or motivation is required to make a rejection under 35 U.S.C. § 103?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Appellant's Invention

1. According to Appellant:

> The present invention relates in general to electronic systems in which memories are used for data storage, as well as program storage. It also relates to uniprocessor and multiprocessor systems, in computer, communication and consumer markets. In particular is described a memory architecture for fixed, as well as variable packet lengths.

(Spec. ¶ [0001]).

2. The present inventive concepts are embodied in a switch comprising a plurality of ports for exchanging data words of a predetermined word-width, or variable word-width, and a shared-memory for enabling the exchange of data between first and second ones of the ports. (Spec. ¶ [0010]).

3. The word-width can also be programmed (variable wordwidth) so that multiple protocols can share the same memory through the intervention of a memory controller. (Spec. ¶ [0010]).

4. In one embodiment, the shared-memory includes an array of memory cells arranged as a plurality of rows, and a single column having a width equal to the predetermined word-width. (Spec. ¶ [0010]).

5. The shared-memory further includes circuitry for writing a selected data word presented at the first one of the data ports to a selected row in the array during a first time period and for reading the selected data

word from the selected row during a second time period to the second one of the ports. (Spec. ¶ [0010]).

6. In one embodiment, the shared-memory includes an array of memory cells arranged as a plurality of rows and a single column having a width equal to the predetermined word-width. (Spec. ¶ [0012]).

7. In another embodiment, column groups in a given row can be selected randomly, where each of the column groups has a predetermined width from a few bytes up to 4 K bytes. (Spec. ¶ [0012]).

8. In another embodiment, the shared memory comprises a plurality of banks, each having an array of memory cells arranged as a plurality of rows and multiple "column groups". The banks also include respective row decoders and "column group" decoders for appropriate access of a given packet. (Spec. ¶ [0014]).

9. Unlike traditional DRAM's where any single column can be selected, in this invention, one "column group" of any given row can be selected. Within any given row, such groups can vary from 1 to 256, based on realities (manufacturable at a cost the market is willing to accept) of practical integrated circuits. (Spec. ¶ [0014]).

10. FIG. 2B illustrates an embodiment where "column groups" can be accessed in the same row of a bank. For example, the minimum wordwidth can be 20 bytes (160 bits), instead of 48 bytes (384 bits) for FIG. 2A. There can be 4, 8, 16 or 32 groups of "20 bytes" in a given row. Appropriate address generation by the controller accesses them appropriately. (Spec. ¶ [0049]).

Appellant's Admissions

11. The Asynchronous Transfer Mode (ATM) protocol is "broadly accepted" in the art. (Spec. ¶ [0003]).

12. It is known in the art to use parity. (Spec. ¶¶ [0004] and [0009]).

13. It is known in the art to use shared-memory switches for packet switching where the user part of each cell is received through a corresponding port and stored in memory. In accordance with a corresponding timing protocol, these data are accessed through a second designated port to complete the switching of the user part of the packet. (Spec. ¶ [0008]).

14. Current shared-memory switches are constructed using static random access memory (SRAM) devices and dynamic random access devices (DRAM). (Spec. ¶ [0009]).

15. A need has arisen for a shared-memory switch which has the high performance of an SRAM and the lower cost and reduced power consumption of a DRAM. RLDRAM I/II.TM., FCRAM.TM., DDRSDRAM are some of the recent DRAM's that are trying to serve these requirements. (Spec. ¶ [0009]).

Joffe

16. The Examiner found that Joffe discloses a switch/system comprising ports for exchanging data between resources, and shared memory (see Abstract, Figs. 1 and 2, col. 1 lines 13-19) comprising an array of cells arranged as rows and a single column having a width equal to a

predetermined word width (Figs. 1 and 2, the shared memory having a single column having a word width of k x m bits, see col. 2 lines 7-29). (October 20, 2006, Non-final Rej. 4).

17. The Examiner found that Joffe discloses circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port (see col. 1 lines 53-64 and col. 2 lines 30-49); converts from initial bit-width to predetermined width (k to k x m). (Id. at 4-5).

18. The Examiner found that an artisan would have recognized the array of Joffe as a random access array of read/write classification. (Id. at 5).

19. The Examiner found that Joffe describes a data format using data along with parity (see col. 2 lines 52-57). (Id. at 7).

20. The Examiner found that parity is one type of overhead associated with data. (Id. at 7).

21. The Examiner found that the system of Joffe has the capability of having bit widths of 48 and 384 as recited (by way of the k and the k x m bit widths). (Id. at 7).

22. Joffe describes that shared memories are connected to multiple devices. (Col. 1, ll. 7-11).

23. Joffe teaches that it is known to use Asynchronous Transfer Mode (ATM) in a shared memory switch. (Col. 8, ll. 63-65).

24. Joffe teaches that it is known that a shared memory can be 384-bits wide so as to accommodate 48-bytes. (Col. 9, ll. 4-6).

Mathur

25. The Examiner found that:

> Mathur discloses a switch/system comprising ports for exchanging data (see Abstract, Fig. 2), and shared RAM memory comprising an array of cells arranged as rows and a single column having a width equal to a predetermined word width (Figs. 2 and 3, memory 20 having a single column since a column can be defined as the width of the entry for a single packet, such as packets 3 and 6 in Fig. 9; alternatively, memory 20 has a single column such as col. 1 or cols. 1-2 in Fig. 9), circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port (see Figs. 6 and 7, also in general col. 1 line 55 to col. 2 line 11, col. 4 lines 31-44, col. 5 lines 56-61, which states that column address is not required, supporting the assertion that the memory may be thought of as a single column, also col. 11 lines 44-56).

(October 20, 2006, Non-final Rej. 5).

26. The Examiner found that Mathur discloses buffers converting the bit-widths (see col. 6 lines 36-65). (Id. at 5).

27. The Examiner found that in Mathur each packet inherently contains certain bit width and associated overhead. (Id. at 5).

28. The Examiner found that Mathur discloses available and used address tables (tables 60 and 80 respectively, one each for each port, see Figs. 6 and 7, see col. 9 lines 8-25 and col. 10 lines 1-15). (Id. at 6).

29. The Examiner found that Mathur discloses a buffer at each port assembling the data stream as recited (see col. 6 lines 36-65). (Id. at 6).

30. The Examiner found that Mathur's memory 20 may be considered a plurality of banks (as vertically divided for ports as shown in Fig. 9). (Id. at 6).

31. The Examiner found that the input port table in Mathur operates as a FIFO. (Id. at 6).

32. The Examiner found that an initial bit width 48, a predetermined bit width of 384, an ATM format, and a DDR data interface were all well known at the time of the invention. (Id. at 8).

33. Mathur describes that switches are connected to network elements and that the network elements comprise workstations and LANs. (Col. 1, ll. 18-63).

34. Mathur teaches that it is known to include a destination along with the message in a packet. (Col. 4, ll. 12-15).

35. Mathur teaches that address table 80 acts as a simple FIFO or queue. (Col. 10, ll. 7-8).

36. Mathur teaches that his invention's architecture allows for scalability of the design such that number of ports, memory size, and the bus width can be scaled and optimized for the application. (Col. 13, ll. 13-15).

PRINCIPLES OF LAW

Burden on Appeal

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)). *See also Hyatt v. Dudas*, 492 F.3d 1365, 1369 (Fed. Cir. 2007) ("As

we explained in *In re Oetiker*, the prima facie case is merely a procedural device that enables an appropriate shift of the burden of production.") *See Id.* ("Once the applicant is so notified, the burden shifts to the applicant to rebut the prima facie case with evidence and/or argument.")

For a rejection under § 102, Appellant may sustain this burden by showing that the prior art reference relied upon by the Examiner fails to disclose an element of the claim. It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1457 (Fed. Cir. 1984).

35 U.S.C. § 102

"For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. These elements must be arranged as in the claim under review, but this is not an "ipsissimis verbis" test." *In re Bond*, 910 F.2d 831, 832-33 (Fed. Cir. 1990) (citations omitted).

"To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.' Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (citations omitted).

35 U.S.C. § 103

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 127 S. Ct. at 1734 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *id.* at 1739, and discussed circumstances in which a patent might be determined to be obvious without an explicit application of the teaching, suggestion, motivation test.

In particular, the Supreme Court emphasized that "the principles laid down in *Graham* reaffirmed the 'functional approach' of *Hotchkiss*, 11 How. 248." *KSR* at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966) (emphasis added)), and reaffirmed principles based on its precedent

that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The Court explained:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 1740. The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.*

Under this framework, once an Examiner demonstrates that the elements are known in the prior art and that one of ordinary skill could combine the elements as claimed by known methods and would recognize that the capabilities or functions of the combination are predictable, then the Examiner has made a prima facie case that the claimed subject matter is likely to be obvious. The burden then shifts to the Appellant to show that the Examiner erred in these findings or to provide other evidence to show that the claimed subject matter would have been nonobvious.

"[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR.*, 127 S. Ct. at 1741 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Claim Construction

"Our analysis begins with construing the claim limitations at issue." *Ex Parte Filatov*, No. 2006-1160, 2007 WL 1317144, at *2 (BPAI 2007).

"The Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582 (Fed. Cir. 1994) (citing *In re Gulack*, 703 F.2d 1381, 1385 (Fed. Cir. 1983)). "Claims must be read in view of the specification, of which they are a part." *Markman v. Westview Instruments, Inc.,* 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc). "[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)).

ANALYSIS

Issue (1)

Appellant argues that the Examiner has erred because the claims are definite as required under 35 U.S.C. § 112, second paragraph. We agree.

We have reviewed Appellant's Specification and the claims on appeal. Although we find the claims on appeal to be broad, we conclude that there is no basis for holding these claims indefinite.

Issue (2)

Appellant repeatedly asserts (15 times) that the Examiner has erred in rejecting claims 1-21 because "the Examiner has not provided . . . objective evidence" to show claimed features (e.g., App. Br. 11) and has rejected other features "without providing any evidence" (e.g., App. Br. 16). We disagree.

The Examiner has rejected claims 1-21 based on the Joffe and Mathur references. The Examiner has made numerous specific findings of fact with regard to Joffe and Mathur (see FF 16-21 and 25-32). Joffe and Mathur also teach numerous additional claimed features (see FF 22-24 and 33-36). Appellant also has made numerous prior art admissions (see FF 11-15).

We find that Joffe and Mathur provide significant evidence to support the Examiner's findings and conclusions. We conclude that Appellant's repeated contentions that the "the Examiner has not provided . . . objective evidence" to show claimed features and has rejected other features "without providing any evidence" are wholly without merit.

Issue (3)

Appellant repeatedly asserts (27 times) that there is no language in a cited passage of either Joffe or Mathur to show a particular feature of a particular claim (e.g., App. Br. 8). We begin with several general observations. First, such assertions are of limited value as the rejections before us are based on the entirety of the two references, not just the cited

passages. Second, anticipation is not an "ipsissimis verbis" test. Third, most of these assertions are followed by boilerplate statements that do not present arguments to support the assertions. In such cases, Appellant is merely arguing that on its face the Examiner's particular rejection is in error. We address such assertions accordingly.

Claims 1 and 16 - Joffe - Anticipation

Appellant asserts that there is no language in the cited passages of Joffe to show the following features of claims 1 and 16: (a) an array of memory cells arranged as a plurality of rows and a single column, (b) the single column having a width equal to a predetermined word-width, (c) writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined word-width during a first time period, and (d) reading the selected data as a word of the predetermined word-width from the selected row during a second time period (App. Br. 7-9). "Thus, Joffe does not disclose all of the limitations of claims 1 and 16." (App. Br. 9).

The Examiner found that Joffe teaches these features. (FF 16-17). We have reviewed these findings of the Examiner and do not find them to be in error on their face which is the essence of the assertions by Appellant.

Claims 2 and 17 - Joffe - Anticipation

Appellant asserts that there is no language in the cited passage of Joffe to show the following feature of claims 2 and 17: (a) a buffer associated with each port for converting words of data from an initial bit-width to the predetermined bit width (App. Br. 10). "Thus, Joffe does not disclose all of the limitations of claims 2 and 17." (App. Br. 10-11).

The Examiner found that Joffe teaches this feature at column 2, lines 7-29. (FF 16 and October 20, 2006, Non-final Rej. 4-5). We have reviewed these findings of the Examiner and do not find them to be in error on their face which is the essence of the assertion by Appellant. We particularly note the Examiner cited passage of Joffe at column 2, lines 17-24.

Claim 7 - Joffe - Anticipation

Appellant asserts that "Joffe does not disclose 'wherein said array comprises an array of random access memory cells of a read/write classification' as recited in claim 7." (App. Br. 11).

The Examiner found that Joffe teaches this feature. (FF 18). We have reviewed this finding of the Examiner and do not find it to be in error on its face which is the essence of the assertion by Appellant.

Claim 17 - Joffe - Anticipation

Appellant asserts that "Joffe does not disclose 'wherein data are exchanged through said ports as streams of data words of an initial word-width' as recited in claim 17 (App. Br. 11).

The Examiner found that Joffe teaches this feature at column 2, lines 7-29. (October 20, 2006, Non-final Rej. 4-5). We have reviewed these findings of the Examiner and do not find them to be in error on their face which is the essence of the assertion by Appellant. We again particularly note the Examiner cited passage of Joffe at column 2, lines 17-24.

Claim 3 - Joffe - Obviousness

Appellant asserts that "Joffe does not teach or suggest 'wherein said predetermined word-width is equal to a bit-width of certain bit width and associated overhead' as recited in claim 3" (App. Br. 31).

The Examiner found that Joffe teaches using overhead in the form of parity. (FF 19 and 20). We have reviewed this finding of the Examiner and do not find it to be in error on its face which is the essence of the assertion by Appellant. We also note Appellant admits that parity is known. (FF 12). In fact, we believe this admission by Appellant to be the only item in Appellant's Specification which reasonably corresponds to overhead.

Claim 4 - Joffe - Obviousness

Appellant asserts that "Joffe does not teach or suggest 'wherein said initial bit-width is 48 bits and said predetermined word-width is 384 bits' as recited in claim 4" (App. Br. 32). Appellant goes on to traverse this and argue that the Examiner must provide a basis in fact and/or technical reasoning to support this finding.

The Examiner found that Joffe has an inherent capacity to have the 48 and 384 bit structure of claim 4. (FF 21 and October 20, 2006, Non-final Rej. 7). We have reviewed this finding of the Examiner and do not find it to be in error on its face which is the essence of the assertion by Appellant. We also note that Joffe teaches that 384-bit wide shared memory is known. (FF 24). Since Joffe's k and m are integers such that (k x m) bits can equal 384, we conclude that an artisan would recognize that m can be any integer that divides evenly in to 384, and that the value 48 qualifies as such an integer.

Claims 1 and 16 - Mathur - Anticipation

Appellant asserts that the Examiner erred in that the Examiner provided no basis for construing the term "column" such that Mathur's memory 20 can be view alternatively as a single column or plural single columns. (FF 25). We disagree.

Appellant's own Specification provides the basis for this understanding of the term. A single physical memory array (e.g., Fig. 2A and 2B) can be viewed as a single column or plural column groups depending on the needs of the user. (FF 6-9). Additionally, as written, Appellant's claims 1 and 16 merely require "an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width." Nothing in this language or the remainder of the claims requires that the memory operate continuously in the single column mode. That is, the language of these claims does not preclude the system shown in Mathur's figure 9 where the word-width is variable, so long as some of the words span the entire memory array. Stated differently, we see nothing in the language of these claims that precludes Appellant's own variable wordwidth embodiment. (FF 1-3).

Appellant also asserts that there is no language in the cited passages of Mathur to show the following features of claims 1 and 16: (a) circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined-word width, (b) circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined-word width during a first time period, (c) reading the selected data as a word of the predetermined word-

width, (d) reading the selected data as a word of the predetermined word-width from the selected row, (e) reading selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined word-width during a second time period, and (f) reading the selected data as a word of the predetermined word-width from the selected row during a second time period for output at the second one of the ports. (App. Br. 15-16). "Thus, Mathur does not disclose all of the limitations of claims 1 and 16." (App. Br. 16).

The Examiner found that Mathur teaches these features. (FF 25). We have reviewed these findings of the Examiner and do not find them to be in error on their face which is the essence of the assertions by Appellant.

Claim 8 - Mathur - Anticipation

Appellant asserts that there is no language in the cited passages of Mathur to show numerous features of claim 8. (App. Br. 16-20).

The Examiner found that Mathur teaches these features. (FF 25-30). We have reviewed these findings of the Examiner and find them to be in error on their face as to two findings. First, although the Examiner correctly found that Mathur's memory 20 is a memory bank (FF 25), Appellant correctly contends that the Mathur's memory 20 cannot be reasonably viewed as "a plurality of banks" as required by claim 8 (App. Br. 17-18). Second, although the Examiner correctly found that Mathur teaches address tables for writing and reading (FF 28), Appellant correctly contends that Mathur does not teach a plurality of each table as required by claim 8 (App. Br. 19-20). We find the remainder of the Examiner's findings with regard to claim 8 to be correct.

We find that the difference between claim 8 and the prior art shown in Mathur is the plurality of banks and tables required by claim 8. However, we conclude that using such pluralities would have been obvious because Mathur explicitly provides a suggestion that his invention is scalable. (FF 36).

We vacate the Examiner's conclusion that Mathur anticipates claim 8 and substitute our own conclusion that claim 8 is unpatentable under 35 U.S.C. § 103 as being obvious over Mathur.

Claims 2 and 17 - Mathur - Anticipation

Appellant asserts that there is no language in the cited passage of Mathur to show a buffer associated with each port (App. Br. 21).

The Examiner found that Mathur teaches this feature. (FF 29). We have reviewed this finding of the Examiner and do not find it to be in error on its face which is the essence of the assertions by Appellant. The Appellant appears to be arguing that term "associated" precludes the buffer being inside the port as shown in Mathur. We find this assertion to be without merit.

Claim 3 - Mathur - Anticipation

Appellant asserts the Examiner erred because the use of a certain bit width and "overhead" (e.g., parity) is not well known in the art (App. Br. 22). We disagree. This argument cannot show Examiner error because the rejection is based on a finding that these features are inherent to the Mathur system. Appellant does not argue otherwise.

Claim 6 - Mathur - Anticipation

Appellant asserts that there is no language in the cited passages of Mathur to show the following features of claim 6: (a) a table for storing addresses already used for writing data, and (b) a table for storing addresses already used for writing data to selected rows in the array. (App. Br. 22-23). "Thus, Mathur does not disclose all of the limitations of claim 6." (App. Br. 23).

The Examiner found that Mathur teaches these features. (FF 27). We have reviewed these findings of the Examiner and do not find them to be in error on their face which is the essence of the assertions by Appellant.

Claim 10 - Mathur - Anticipation

Appellant asserts that Mathur does not show that input-port table (element 60) is a FIFO buffer as found by the Examiner (App. Br. 23) (FF 31). We agree. We find that Mathur is silent as to buffer being a FIFO.

We find that the differences between claim 10 and the prior art shown in Mathur are the plurality of banks and tables required by claim 8 and the FIFO required by claim 10. However, we have already concluded that using such pluralities would have been obvious because Mathur explicitly provides a suggestion that his invention is scalable. (FF 36). We further conclude that use of a FIFO buffer would have been obvious because Mathur explicitly provides a teaching that related table 80 is a FIFO (FF 35) which is a suggestion that similar table 60 could also be a FIFO.

We vacate the Examiner's conclusion that Mathur anticipates claim 10 and substitute our own conclusion that claim 10 is unpatentable under 35 U.S.C. § 103 as being obvious over Mathur.

Claims 11-15 - Mathur - Anticipation

Appellant asserts that the Examiner erred because "the Examiner has not cited to any passage in Mathur as allegedly disclosing the claim limitations of claims 11-15." (App. Br. 24). We agree in part.

Appellant assertion as to claims 11 and 12 relies on a mistaken belief that the Examiner is required to explicitly point out every individual feature in the claims even where the cited reference (or passages) clearly teach each feature. For example, the tables of Mathur's columns 9-10 would be recognized as a random access memory that performs read and write operations as required by claim 11; and column 6, line 60, of Mathur, clearly teaches the randomly assessable memory required by claim 12.

Solely because these claims depend from claim 8, we vacate the Examiner's conclusion that Mathur anticipates claims 11 and 12 and substitute our own conclusion that claims 11 and 12 are unpatentable under 35 U.S.C. § 103 as being obvious over Mathur.

As to claims 13-15, we agree with Appellant to the extent that because Mathur fails to teach plural banks as discussed *supra*, Mathur cannot therefore teach the relationships among the banks and ports.

We find that the differences between claim 13-15 and the prior art shown in Mathur are the plurality of banks and tables required by claim 8 and the port to banks relationships required by claims 13-15. However, we have already concluded that using such pluralities would have been obvious because Mathur explicitly provides a suggestion that his invention is scalable. (FF 36). Moreover, we find the duplication of banks and tables is nothing more than a "predictable use of prior art elements according to their

established functions" and, as such, is not a patentable distinction. *KSR*, 127 S. Ct. at 1740. We further conclude that use of the claimed relationships would have been obvious because Mathur explicitly provides suggestions that (a) each selected port can correspond to a selected memory area as required by claims 13 and 14 (see Mathur's figure 9), and (b) the number of ports in Mathur is greater than the number of banks (one) as required by claim 15 (see figures 2 and 3). We also find the claim 14 limitation "in a selected order" to be inherent to any memory operation.

We vacate the Examiner's conclusion that Mathur anticipates claims 13-15 and substitute our own conclusion that claims 13-15 are unpatentable under 35 U.S.C. § 103 as being obvious over Mathur.

Claim 20 - Mathur - Anticipation

Appellant asserts that the Examiner erred because "the Examiner has not cited to any passage in Mathur as allegedly disclosing the above-cited claim [20] limitation." (App. Br. 25). We disagree.

Appellant assertion as to claim 20 relies on a mistaken belief that the Examiner is required to explicitly point out every individual feature in the claims even where the cited reference (or passages) clearly teach each feature. The workstations and digital data networks required by claim 20 are clearly taught by column 1 of Mathur. (FF 33).

Claims 4, 9, 18, and 19 - Mathur - Obviousness

Appellant asserts that the Examiner erred because an initial bit width 48, a predetermined bit width of 384, or an ATM format are not well known in the art as the Examiner found (App. Br. 34-35). We disagree.

The Examiner found that these features were all well known at the time of the invention. (FF 32). Given the Examiners findings (FF 21), our findings (FF 23-24), and Appellant's admission (FF 11) we reach the same conclusion that these claims are obvious.

As to claim 9, solely because this claim depends from claim 8, we vacate the Examiner's conclusion and substitute our own conclusion that claim 9 is unpatentable under 35 U.S.C. § 103 as being obvious over Mathur for the reasons discussed *supra* with regard to claim 8.

Claim 21 - Mathur - Obviousness

Appellant asserts that the Examiner erred because a data interface comprising, for example DDR, is not well known in the art as the Examiner found (App. Br. 36-37). We disagree.

The Examiner found that this feature was well known at the time of the invention. (FF 32). Given Appellant's admission (FF 15) that use of DDRSDRAM (SDRAM using DDR) was known in the art we reach the same conclusion that this claim is obvious.

Issue (4)

Appellants contend that the Examiner erred in rejecting claims 4, 9, 18, 19, and 21 under 35 U.S.C. § 103(a) as being unpatentable because the Examiner has not provided a proper teaching, suggestion, or motivation to modify Mathur (App. Br. 32-37). We disagree.

Appellant's contention that the Examiner is required to provide a suggestion or motivation to modify Mathur is without merit. Rather, the references we find before us are in the same field of computer network

switching as Appellant's invention, and the Examiner has demonstrated that the claimed elements were known in the prior art and that one of ordinary skill could have modified the elements as claimed by known methods and would have recognized that the capabilities or functions of the combination were predictable. *See KSR*, 127 S. Ct. 1727.

We conclude that based on the strength of Examiner prima facie showing, nothing in Appellant's arguments is sufficient to rebut a final conclusion of obviousness with regards to these claims.

Therefore, for the reasons above, Appellant has not established that the Examiner erred with respect to this rejection of claims 4, 9, 18, 19, and 21 under § 103.

NEW GROUNDS OF REJECTION

35 U.S.C. § 103

Using our authority under 37 C.F.R. § 41.50(b), we have rejected claims 8-15 under 35 U.S.C. § 103 as discussed *supra*.

37 C.F.R. § 41.50(b)

37 C.F.R. § 41.50(b) provides that, "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellant, *WITHIN TWO MONTHS FROM THE DATE OF THE DECISION*, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of proceedings (37 C.F.R. § 1.197 (b) as to the rejected claims:

> (1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected,

> or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner …
>
> (2) Request rehearing. Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record …

37 C.F.R. § 41.52(a)

Regarding the affirmed rejection, 37 C.F.R. § 41.52(a)(1) provides "Appellant may file a single request for rehearing within two months from the date of the original decision of the Board." Should Appellant elect to prosecute further before the Examiner pursuant to 37 C.F.R. § 41.50(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the Examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If Appellant elects prosecution before the Examiner and this does not result in allowance of the application, abandonment, or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

CONCLUSION OF LAW

(1) Appellant has failed to establish that the Examiner erred in rejecting claims 1, 2, 7, 16, and 17 as being unpatentable under 35 U.S.C. § 102(b) over Joffe.

(2) Appellant has failed to establish that the Examiner erred in rejecting claims 3 and 4 as being unpatentable under 35 U.S.C. § 103(a) over Joffe.

(3) Appellant has failed to establish that the Examiner erred in rejecting claims 1-3, 5-7, 16, 17, and 20 under 35 U.S.C. § 102(b) as being anticipated by Mathur.

(4) Appellant has failed to establish that the Examiner erred in rejecting claims 4, 18, 19, and 21 as being unpatentable under 35 U.S.C. § 103(a) over Mathur.

(5) Appellant has established that the Examiner erred in rejecting claims 8 and 10-15 under 35 U.S.C. § 102(b) as being anticipated by Mathur. However, we reject these claims anew as being unpatentable under 35 U.S.C. § 103(a) over Mathur.

(6) Appellant has established that the Examiner erred in rejecting claim 9 as being unpatentable under 35 U.S.C. § 103(a) over Mathur. However, we reject claim 9 anew as being unpatentable under 35 U.S.C. § 103(a) over Mathur.

(7) Claims 1-21 are not patentable.

DECISION

The Examiner's rejection of claims 1-21 under 35 U.S.C. § 112, second paragraph, is reversed.

The Examiner's rejections of claims 1-7 and 16-21 based on Joffe and Mathur are affirmed.

The Examiner's rejections of claims 8-15 based on Mathur are vacated.

We reject claims 8-15 under 35 U.S.C. § 103(a) based on Mathur.

Since we have entered a new rejection, our decision is not a final agency action.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART
VACATED-IN-PART
37 C.F.R. § 41.50(b)

pgc

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